WHAT IS CLAIMED IS

1. An isolated high-voltage LDMOS transistor comprising:

a P-substrate;

a first diffusion region and a second diffusion region having N conductivity-type, wherein said first diffusion region and said second diffusion region form a N-well in said P-substrate, wherein said first diffusion region forms an extended drain region;

a drain diffusion region, for forming a drain region, said drain diffusion region having N+ conductivity-type, wherein said drain region is disposed in said extended drain region;

a third diffusion region, for forming a P-well separately located in said extended drain region of said N-well, said third diffusion region having P conductivity-type;

a source diffusion region, for forming a source region, said source diffusion region having N+ conductivity-type, wherein a conduction channel is formed through said N-well, wherein said conduction channel connects said source region and said drain region;

a contact diffusion region, for forming a contact region, said contact diffusion region having P+ conductivity-type; and

a fourth diffusion region, for forming an isolated P-well to prevent breakdown, said fourth diffusion region having P conductivity-type, wherein said isolated P-well is located in said second diffusion region in order to enclose said source region and said contact region, wherein said N-well created by said second diffusion region produces a low-impedance path for said source region, wherein said N-well generated by said second diffusion region restricts a transistor current flow between said drain region and said source region.

2. The isolated high-voltage LDMOS transistor of claim **1**, wherein said extended drain region and said drain diffusion region form a drain electrode.

3. The isolated high-voltage LDMOS transistor of claim **1**, wherein said isolated P-well, said source diffusion region, and said contact diffusion region form a source electrode.

4. The isolated high-voltage LDMOS transistor of claim **1**, wherein said N-well is established from said drain electrode to said source electrode.

5. The isolated high-voltage LDMOS transistor of claim **1**, wherein said P-well splits said N-well.

6. The isolated high-voltage LDMOS transistor of claim **1** further comprising:

a thin gate oxide and a thick field oxide formed on said P-substrate;

a polysilicon gate electrode, for controlling said transistor current flow in said conduction channel, wherein said polysilicon gate electrode is placed above portions of said thin gate oxide and said thick field oxide;

a drain-gap, for maintaining a space between said drain diffusion region and said thick field oxide;

a source-gap, for maintaining a space between said thick field oxide and said isolated P-well, wherein the placement of said drain-gap and said source-gap substantially increases the breakdown voltage of said isolated high-voltage LDMOS transistor;

a silicon dioxide insulation layer, covering said polysilicon gate electrode and said thick field oxide;

a drain metal contact, having a metal electrode for contacting with said drain diffusion region; and

a source metal contact, having a metal electrode for contacting with said source diffusion region and said contact diffusion region.

7. The isolated high-voltage LDMOS transistor of claim **1** further comprising:

a drain bonding pad, for said drain electrode, wherein said drain bonding pad is connected to said drain metal contact;

a source bonding pad, for said source electrode, wherein said source bonding pad is connected to said source metal contact; and

a gate bonding pad, connected to said polysilicon gate electrode.

8. The isolated high-voltage LDMOS transistor of claim **1**, wherein said P-well splits said extended drain region of said N-well to form a split junction-field in said N-well, wherein said split N-well and said P-well deplete a drift region.